REMARKS

This responds to the Office Action dated on March 23, 2005. Claims 47, 55, 67 and 76 are amended, no claims are canceled, and no claims are added; as a result, claims 47-50, 55, 60, 61, 67-69, and 76-78 are now pending in this application.

Double Patenting Rejection

Claims 47-50, 55, 60, 61, 67-69, and 76-78 were rejected under the judicially created doctrine of obvious-type double patenting as being unpatentable over claims 1, 8-11, and 14-18 of Ahn et al. (U.S. Patent No. 6,821,802) in view of Horiuchi (JP 05129666). Applicant does not admit that the claims are obvious as asserted in this rejection. However, Applicant will consider filing a Terminal Disclaimer when all claims are indicated to be otherwise allowable.

§103 Rejection of the Claims

Claims 47, 55, 66, and 76 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beaman et al. (U.S. Patent No. 5,371,654) in combination with Horiuchi (JP 05129666). Applicant respectfully traverse this rejection.

The cited Horiuchi reference discloses a Peltier element 18 made of small plates of semiconductor 24 formed in a prismatic shape, and small rectangular plates of metal 20 and 22, arranged between the back surface of the IC 28 and the outside portion of the IC package, the cap 12. The Peltier element is directly in contact with the back surface of the IC 28 and with the inner surface of the metal cap 12 and held together by polyimide clamping layer 26 around the lateral sides of the group of elements.

The cited Beaman reference discloses a multi-level circuit board having IC and other electronic devices 36 and 38, on one side of each of the multiple circuit board layers 8, each of which has multiple layers of circuitry and interconnect 14, and having no clearance for attachment of Peltier elements on the electronic devices due to the stack nature of the device. The individual circuit boards 8 are formed of elastomeric materials or solid materials having elastomeric layers so that when the device stack is compressed the electrical interconnects are held closed.

Applicant respectfully submits that the suggested combination of references of Beaman in view of Horiuchi fails to describe or suggest at least the claim language "...*wherein the Peltier element is physically attached to an insulating layer on a back portion of the flip chip, and has a connection lead electrically connecting one surface of the Peltier element to the back portion of the flip chip, and a second connection lead electrically connecting another surface of the Peltier element to a voltage source* ...", as recited in independent claim 47, as amended herein. The Peltier element of Horiuchi is formed of prismatic pieces of metal held together by the cap 12 of the inner portion of the IC package 14, and is not attached to an insulating layer on the IC 28. The Peltier element in Horiuchi does not have connection leads to either the back portion of the IC 28 or to a voltage source. Similar reasons pertain to the other independent claims 55, 67 and 76, which contain similar language.

Applicant respectfully submits that the suggested combination of the cited Beaman reference with Horiuchi does not describe or suggest the claimed feature of "...*coupling a semiconductor chip to each of the opposing sides of the silicon interposer* ...", as recited in claim 55, as amended herein. This is true since the connections of the semiconductor chips 36 and 38 are either to the same side of a circuit board 8, or are on different ones of the circuit boards 8, and are not on opposite sides of the printed circuit boards 8, which are also not interposers. The inter chip connections in Beaman are through the printed circuit boards 8, to the electrical interconnection means mini-interposer 49, and thus to another printed circuit board 8 and to the other IC 36. Neither Beaman nor Horiuchi disclose or suggest the semiconductor chips connecting to opposing sides of the interposer as claimed in the present application.

Applicant respectfully submits that one of ordinary skill in the art would not be motivated to combine the Peltier device inside a metal package cap of Horiuchi to the Beaman multiple circuit board, since such a combination would result in a arrangement that is against the described purpose of the Beaman device. Specifically, such an arrangement of a Peltier device over the top surface of the Beaman ICs would not reduce the electrical signal propagation distances, because the increased height would increase the board 8 to board 8 spacing and thus increase system wiring lengths and delay.

The other rejected claims are felt to be in patentable condition for similar reasons to those given above. In view of the above noted claim amendments and discussion, Applicant requests that this rejection be reconsidered and withdrawn.

Claims 48-50, 60-61, 68, 69, 77, and 78 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beaman et al. (U.S. Patent No. 5,371,654) and Horiuchi (JP 05129666) as applied to claims 47, 55, 67, and 76 and further in combination with Wenzel et al. (U.S. Patent No. 6,150,724). Applicant respectfully traverse this rejection.

The features of Beaman and Horiuchi have been discussed above. The cited reference of Wenzel is used in the outstanding Office Action to show that connecting microprocessors to memory chips is known.

Applicant respectfully submits that the suggested combination of references has the same failures as those discussed above with reference to the previous rejection. Specifically, that the Beaman reference does not disclose the claimed feature of "*...coupling a semiconductor chip to each of the opposing sides of the silicon interposer ...*", as recited in claim 55, as amended herein, and with similar language in the other independent claims. The Beaman reference uses an electrical interconnection means mini-interposer 49 to connect two printed circuit boards 8, and does not disclose the semiconductor chips connecting to opposing sides of the interposer as claimed in the present application. Applicant further submits that the Peltier element array 18 of Horiuchi has a different arrangement as noted above and as compared to the present Peltier element 160 of Applicant's figure 1A, or elements 127, 128 and 129 forming Peltier element 160 in figure 1B. There is no cap in the present invention to hold the multiple pieces of the Peltier device together and there are no connection leads. Applicant submits that there is no motivation given to make the suggested combination since the space available above the IC chips in Beaman would not allow a heatsink or Peltier device to be attached.

The dependent claims are felt to be in patentable condition at least as depending from base claims shown above to be patentable. Applicant requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 25 July '05

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 25 day of July, 2005.

Tina Kohut
Name

Signature